

## STRUCTURE AND METHOD FOR FORMING A CAPACITIVELY COUPLED CHIP-TO-CHIP SIGNALING INTERFACE

### TECHNICAL FIELD

The present invention is directed to a system-in-package device, and  
5 more particularly, to a system and method for providing capacitively-coupled signaling  
in a system-in-package device.

### BACKGROUND OF THE INVENTION

Traditional semiconductor integrated circuit technology is commonly  
used to integrate various electronic circuits onto a common semiconductor substrate to  
10 form an electronic system, or subsystem. The traditional approach to integrating  
circuits into a system often has process, manufacturing and design limitations which  
present difficulties when certain electronic circuits are integrated onto a common  
semiconductor substrate. A recently developed integration technology commonly  
referred to as system-in-package (SiP) technology attempts to overcome at least some of  
15 the limitations of traditional semiconductor integration methods by interconnecting  
multiple discrete and individually fabricated semiconductor systems on a common  
substrate and encapsulating the complete system in a common package. Accordingly,  
SiP allows a variety of device technologies to be integrated into a single package that  
would otherwise be difficult and expensive to fabricate using traditional integration  
20 methods. For example, SiP technology has been successfully applied in mixed signal  
applications, where analog and digital components are integrated onto the same chip.  
Such applications typically present noise immunity difficulties, since digital circuit  
switching commonly injects noise into the common substrate, which may corrupt  
sensitive analog signals. As the size of features in devices decreases and clock  
25 frequencies increase, the amount of substrate noise created by digital switching has  
increased dramatically.

As previously mentioned, the multiple discrete systems of a SiP are electrically coupled together to form a system and, as is well known in the art of digital electronics, many of the multiple systems communicate with one another by transmitting digital information in the form of electrical signals. Typically, even  
5 analog-based systems in the SiP generally have analog signals converted into the digital domain. The electrical signals transmitted between the multiple systems generally represent a serial data stream where the data is represented by binary states having discrete levels of amplitude or phase, as well known. Multiple electrical signals are transmitted in parallel to transmit data of a data width, with each signal representing one  
10 bit of the width of data. In transmitting the data, the electrical signal may be distorted by various phenomena, such as noise, signal strength variations, phase shift variations, and the like. Moreover, multiple individual devices generally interact in a SiP, and the various devices may operate at different voltage levels that may cause undesired electrical currents to flow from one system to another, which generally contributes to  
15 excess power consumption. Additionally, the undesired current may be sufficiently large to damage to the devices.

Consequently, SiP devices have employed capacitively coupled signaling between the multiple systems to filter noise from the electrical signals and also prevent current flow between devices operating in different voltage domains. Figure 1  
20 illustrates a capacitively coupled signaling system having a capacitively coupled data bus 100 that is n-bits wide that may be used to transmit data signals D\_OUT0-D\_OUTn. The data bus 100 includes output driver circuits, or transmitters 102 of the transmitting device capacitively coupled through capacitors 106 to input buffer circuits, or receivers 104 at the receiving device. The received data has been represented by the  
25 received data signals D\_IN0-D\_INn. As shown in Figure 1, the data bus 100 has been illustrated as a uni-directional data bus, with the transmitters 102 representing a transmitting device and the receivers 104 representing a receiving device. However, it will be appreciated that the data bus 100 has been illustrated in this manner by way of example, and that the data bus 100 can be a bi-directional data bus as well.

Lower power may be consumed when utilizing capacitively coupled signaling since there is only minimal leakage current between devices. Capacitively coupled signaling is also insensitive to voltage domains, allowing operation without the need for level shifting. Specifically, a capacitively coupled signaling system permits an AC component of a signal to be transferred, while blocking a DC component of the signal. Additionally, circuits designed for protection from electrostatic discharge (ESD) are no longer necessary where the signaling is entirely contained within the SiP device. Circuits dedicated to ESD protection, usually consisting of diode networks in various configurations, add complexity to the terminal regions of a device, and compete for "real estate" on the device substrate. Load requirements on output circuitry can also be relaxed compared with conventional off-die signaling because the need to drive signals external to the device package are eliminated for those signals that remain internal to the SiP device.

In forming capacitively coupled signaling systems, discrete passive components have been used to connect the signal terminals of the different systems, such as discrete capacitors, resistors, and the like. However, when discrete components are used, some of the foregoing advantages associated with a capacitively coupled signaling system are reduced. For example, when a signal pad is wire bonded to a discrete passive component that further extends to another signal pad, parasitic effects are generally introduced. Additionally, when several discrete components are included in a SiP, an increased form factor is generally developed, since the additional components must be accommodated. Passive components can be integrated into each discrete system, thereby avoiding issues with having additional passive components included in the SiP, but even when the passive components are integrated into the SiP, the need to have wires coupling the signal pads of the discrete systems cannot be avoided. As noted above, bonding wires can cause undesirable parasitic loading effects. Therefore, there is a need in the art for an alternative capacitively coupled signaling structure and a method for forming a capacitively coupled structure.

## SUMMARY OF THE INVENTION

The present invention is directed to a system and method for providing capacitively-coupled signaling in a system-in-package (SiP) device. In one aspect, the SiP device includes a first semiconductor device and an opposing second semiconductor device spaced apart from the first semiconductor device, a dielectric layer interposed between the first semiconductor device and the second semiconductor device, a first conductive pad positioned in the first semiconductor device, and a second conductive pad positioned in the second semiconductor device that is configured to capacitively communicate signals from the second semiconductor device to the first semiconductor device. In another aspect, a method of forming a SiP device includes forming a first conductive signal pad on a surface of a first semiconductor device, forming a second conductive signal pad on a surface of a second semiconductor device, and interposing a dielectric layer between the first semiconductor device and the second semiconductor device that separates the first conductive signal pad and the second conductive signal pad.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic view of a capacitively coupled signaling system according to the prior art.

Figure 2 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to an embodiment of the invention.

Figure 3 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to another embodiment of the invention.

Figure 4 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to still another embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention is generally directed to a system-in-package device, and more particularly, to a system and method for providing capacitively-coupled signaling in a system-in-package device. Many of the specific details of certain

embodiments of the invention are set forth in the following description and in Figures 2-4 to provide a thorough understanding of such embodiments. One skilled in the art will understand, however, that the present invention may be practiced without several of the details described in the following description. Moreover, in the description that  
5 follows, it is understood that the figures related to the various embodiments are not to be interpreted as conveying any specific or relative physical dimension. Instead, it is understood that specific or relative dimensions related to the embodiments, if stated, are not to be considered limiting unless the claims specifically state otherwise.

Figure 2 is a partial isometric and cross-sectional view of a capacitively  
10 coupled SiP 200 according to an embodiment of the invention. The SiP 200 includes a first semiconductor device 210 and a second semiconductor device 220 that is spaced apart from the first semiconductor device 210 by a dielectric layer 230. The first semiconductor device 210 includes a signal pad 212 that is coupled to the transmitter 102 that transmits a data signal D\_OUT0 to the signal pad 212. The first semiconductor  
15 device 210 further includes a signal pad 214 that is coupled to the transmitter 102 that transmits a data signal D\_OUT1 to the signal pad 214. In a similar manner, the second semiconductor device 220 includes a signal pad 222 that is coupled to the receiver 104 that transmits a data signal D\_IN0 from the signal pad 222. The second semiconductor device 220 further includes a signal pad 224 that is coupled to the receiver 104 that  
20 transmits a data signal D\_IN1 from the signal pad 224. The pads 212 and 222, and the pads 214 and 224 are positioned within the semiconductor devices 210 and 220 to permit the data signals to be exchanged between the devices 210 and 220 through the dielectric layer 230 by capacitive coupling. Although Figure 2 illustrates only four signal pads that are configured to capacitively transfer signals between the first  
25 semiconductor device 210 and the second semiconductor device 220, it is understood that the capacitively coupled SiP 200 may include more than four similarly configured pads, or as few as two signal pads.

The signal pad 212 of the first semiconductor device 210 and the pad 222 of the second semiconductor device 220 are approximately mutually in alignment,  
30 as shown in Figure 2, so that the capacitive coupling between the semiconductor

devices 210 and 220 may be maximized. Similarly, the pads 214 and 224 are approximately mutually in alignment to maximize capacitive coupling between the semiconductor devices 210 and 220. One skilled in the art will readily appreciate that the pads 212 and 222 may be configured such that the pads 212 and 222 are only in  
5 relative proximity and still achieve capacitive coupling between the devices 210 and 220. In a similar manner, the pads 214 and 224 may also be configured so that the pads 214 and 224 are only relatively proximate to one another.

Still referring to Figure 2, the dielectric layer 230 of the SiP 200 may be comprised of silicon dioxide, silicon nitride, or other alternative dielectric materials that  
10 are deposited on each of the first semiconductor device 210 and second semiconductor device 220. Alternately, and in a particular embodiment, the dielectric layer 230 may be comprised of a passivated layer formed on exposed surfaces of the first semiconductor device 210 and/or the second semiconductor device 220 during fabrication of the semiconductor devices 210 and 220. In either case, the dielectric layers formed on the  
15 first semiconductor device 210 and the second semiconductor device 220 may be combined by adhesive bonding, or by other similar methods, to form the SiP 200 shown in Figure 2. Alternately, and in another particular embodiment, the first semiconductor device 210 and the second semiconductor device 220 may be combined to form the SiP 200 by a low temperature covalent bonding process as disclosed in U.S. Patent No.  
20 6,563,133 B1 to Tong, entitled "Method of Epitaxial-Like Wafer Bonding at Low Temperature and Bonded Structure", which is incorporated by reference herein.

The pads 212 and 214 of the first semiconductor device 210 and the pads 222 and 224 of the second semiconductor device 220 may be formed on the devices 210 and 220 by a variety of well-known methods. For example, the pads 212 and 214, and  
25 the pads 222 and 224 may be formed by depositing a layer of a dielectric material onto the first device 210 and the second device 220, masking the dielectric layers on the devices 210 and 220 and then selectively etching the dielectric layers to form recesses in the dielectric layers. A conductive material may then be deposited into the recesses to form the pads 212 and 214, and the pads 222 and 224. The pads 212, 214 and 222 and  
30 224 may be appropriately sized to achieve a desired degree of capacitive coupling. For

example, and in one particular embodiment, the pads 212, 214, 222 and 224 have a width  $d_1$  of approximately about 30  $\mu\text{m}$ . Further, the transmitters 102 and the receivers 104 may be positioned remotely from the pads 212 and 214 and the pads 222 and 224, respectively, as shown in Figure 2. The transmitters 102 may also be formed  
5 in the first semiconductor device 210 at a location that is proximate to the pads 212 and 214. For example, the transmitters 102 may be formed at a location that is laterally adjacent to the pads 212 and 214. Alternately, the transmitters 102 may be positioned directly below and adjacent to the pads 212 and 214. In a similar manner, the receivers 102 may also be positioned at a location proximate to the pads 222 and 224, which  
10 includes positioning the receivers 102 in positions laterally adjacent to the pads 222 and 224, or directly below the pads 222 and 224.

Figure 3 is a partial isometric and cross-sectional view of a capacitively coupled SiP 300 according to another embodiment of the invention. The SiP 300 includes first and second semiconductor devices 210 and 220, respectively, which are  
15 separated by the dielectric layer 230, as in the previous embodiment. The SiP 300 further includes guard rings 310 laterally spaced apart from the pads 212, 214, 222 and 224. Each of the guard rings 310 is coupled to ground to inhibit capacitive coupling between adjacent signal pads. Accordingly, the guard rings 310 may be formed in the first semiconductor device 210 so that the pads 212 and 214 are circumferentially  
20 enclosed by the guard rings 310. Alternately, the guard rings 310 may only partially enclose the pads 212 and 214, or extend along lateral edges of the pads 21 and 214, as shown in Figure 3. Similarly, the guard rings 310 formed in the second semiconductor device 220 may circumferentially enclose the pads 222 and 224, or they may only partially enclose the pads 212 and 214, or extend along lateral edges of the pads 222 and  
25 224, as described above. Although Figure 3 shows guard rings 310 adjacent to each of the pads 212, 214, 222 and 224, one skilled in the art will appreciate that the guard rings 310 may formed adjacent to only a portion of the signal pads in the first semiconductor device 210 and the second semiconductor device 220, while other signal pads in the devices 210 and 220 are formed without adjacent guard rings 310. Further, the guard

rings 310 may be formed in only one of the first semiconductor device 210 and the second semiconductor device 220.

Still referring to Figure 3, the guard rings 310 may be formed in the exposed surfaces of the first semiconductor device 210 and the second semiconductor device 220 by a variety of well-known processes. For example, the guard rings 310 may be formed in the dielectric material deposited on the first device 210 and the second device 220 by masking the dielectric layer so that the layer may be selectively etched to form recesses in the dielectric layers. A conductive material may then be deposited into the recesses to form the guard rings 310. In one particular embodiment, the guard rings 310 may extend into the first and second devices 210 and 220 to a depth  $d_3$  of approximately about  $0.8\mu\text{m}$ . In another particular embodiment, the guard rings 310 are spaced apart from the signal pads 212, 214, 222 and 224 by a distance  $d_4$  of approximately about  $2\mu\text{m}$ . In still another particular embodiment, the guard rings 310 have a width  $d_5$  of approximately about  $2\mu\text{m}$ .

Figure 4 is a partial isometric and cross-sectional view of a capacitively coupled SiP 400 according to still another embodiment of the invention. The SiP 400 includes first and second semiconductor devices 210 and 220 separated by the dielectric layer 230, as in embodiments described above. The SiP 400 further includes a first ground plane 410 positioned within the first semiconductor device 210 and spaced apart from the pads 212 and 214. The first ground plane 410 may be coupled to the guard rings 310 formed in the first semiconductor device 210 to provide a low impedance path to ground for the guard rings 310. The SiP 400 also includes a ground plane 420 positioned within the second semiconductor device 220 that is spaced apart from the pads 222 and 224. The second ground plane 420 may also be coupled to the guard rings 310 formed in the second semiconductor device 220. The first ground plane 410 and the second ground plane 420 may be formed from either metallic or non-metallic conductive materials, and may be formed within the first device 210 and the second device 220 by various well-known methods. For example, in a particular embodiment, the first ground plane 410 and the second ground plane 420 may be formed by depositing a layer of copper or aluminum on the first and second devices 210 and 220



during fabrication of the devices 210 and 220. Alternately, in another particular embodiment, a layer of heavily doped polycrystalline silicon may be formed within the devices 210 and 220 to form the ground planes 410 and 420. In still another particular embodiment, the first ground plane 410 and the second ground plane 420 are spaced  
5 apart from the respective surfaces of the first semiconductor device 210 and the second semiconductor device 220 by a distance  $d_6$  of approximately about  $1.90\mu\text{m}$ .

The foregoing embodiments of the invention offer numerous advantages over the prior art. For example, the disclosed embodiments generally eliminate the need for electrostatic discharge (ESD) protection in the semiconductor devices comprising  
10 the SiP. Accordingly, the requirement to form additional devices, such as diodes or similar protective devices near the pads on a semiconductor device is eliminated, so that the device area, or "real estate" may be more efficiently utilized.

The foregoing embodiments also generally allow shorter signal paths to be established between the devices in the SiP. Accordingly, signal delay times are  
15 significantly reduced when compared to conventional wire bond or interposer coupling techniques. Undesirable parasitic effects are similarly reduced since the inductance associated with a wire bonding element is largely eliminated. Load requirements are also advantageously reduced since a relatively low capacitive load is present between the devices. As a result, the power requirement is significantly reduced in comparison  
20 to conventional packages, where the devices are required to drive signals off one device, and onto another device. The low capacitive load between the devices further advantageously permits relatively high bandwidth operation between the devices.

Still other advantages are evident in the foregoing embodiments. For example, since the devices are capacitively coupled, the devices may be operated at  
25 different D.C. voltage levels without the requirement for D.C. voltage isolation or D.C. level shifting between the devices. Since the foregoing pad, ground ring and ground plane structures are fabricated near the exterior layers of the devices, the structures may be conveniently formed in the devices by altering only the final steps in the fabrication procedure. Accordingly, the foregoing structures may be economically incorporated  
30 into the devices by altering relatively few semiconductor device masks.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.